A Case for Custom Power Management ASIC

By Cirel Systems

Introduction

The mobile device explosion seems to continue without a pause. The convergence of functionalities on a palm top device is fuelling applications that till yesterday seemed straight from a science fiction story. Several innovations in a wide range of disciplines have enabled this. Innovations in sensors have added a lot of functionality to these portable, handhelds. Touch sensors and stylus are replacing the traditional keyboard and mouse. MEMS microphones are enabling addition of multiple microphones in a device, enabling echo cancellation applications. Improvements in display panels and audio functionalities are making video functionality a given in these devices. And of course, the evolution of 3G and 4G network has enabled high speed data connectivity. The recent revving up of Operating System wars is an indication of how seriously the industry takes this space. It is distinctly possible that these handheld platforms will be the personal computers for everyday use in the near future.

As usual, all good things in life come with at a price. In this case on the price side, power is the biggest one. As more functionality has been added to the devices, the power requirements have increased. As the power requirement grows, the capacity of the battery has to be increased, increasing the space occupied and its weight. This makes the battery one of the bulkiest components in the handhelds.

Process improvements, system architecture improvements etc have helped in keeping the power dissipation under some control. Still it is imperative that no power be wasted in the device. This is the primary function of the power management in the device. Apart from this, it is necessary to keep the cost of the solution low as well as occupy less space.

System requirements

Multiple Voltage / Power Generation

With multiple features added to the device, it is imperative to be able to control the power delivery for each of these functions to help improve the battery life. E.g. if the user is listening to music, it may be possible to switch off the display. Or if the device is in a standby mode, all the added functions except for the wakeup logic should be powered down. Powering down could be done either by controlling the logic or by removing the power to the device totally. The latter is preferred especially in cases where the leakage from the power supply of the function is large. And this is the case in deep sub-micron (DSM) processes which invariably have

to be used to integrate the myriad functions. This brings up the necessity to generate multiple voltage islands that can be independently controlled.

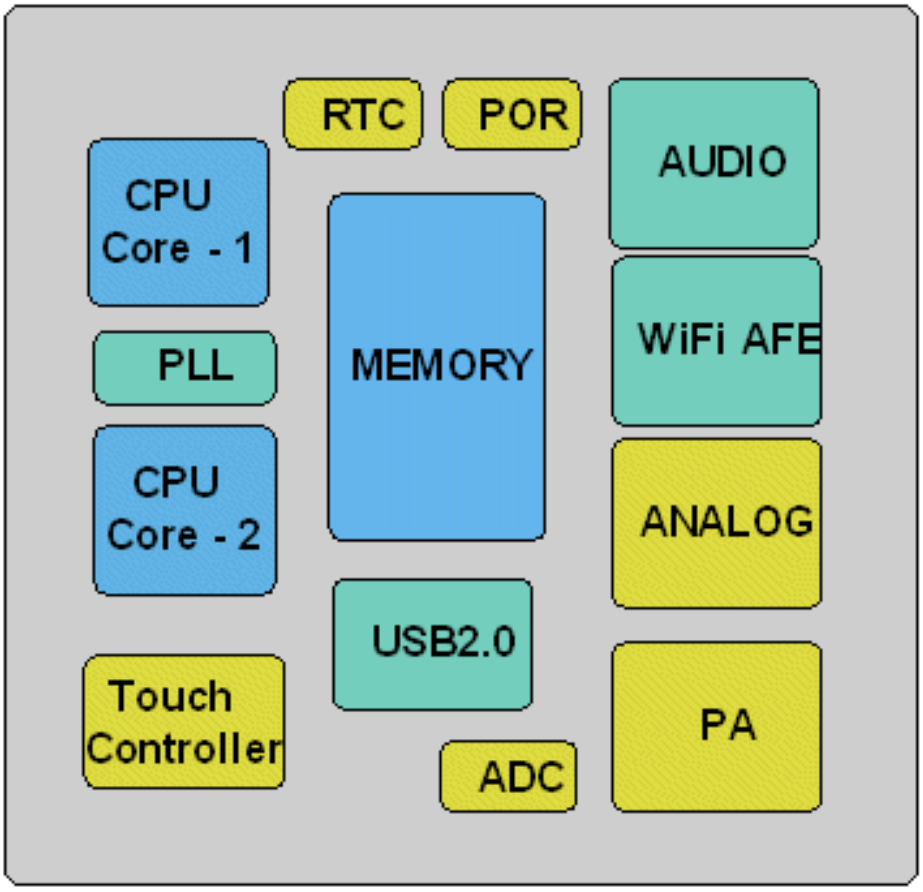

Figure 1: Example of sub systems in a SoC. Power requirements will be different for all these sub systems.

Efficiency

These voltages feed the various sub blocks in the system. Some of these will be around 1V (typically the digital core to reduce the switching power and higher speed of the core devices), some will be 2.5V (typically analog signal processors for better signal quality) and a few even higher (13-15V for a 3 chain LED for backlighting). Li Ion batteries are typically used in these devices, output voltage ranging from 2.7V to 4.2V. Generating the 1V for the core delivery about 500ma to 1A would have to be done by a switching converter (linear converters will dissipate a lot of power). The efficiency of the switching converter depends on the switch size, the operating frequency as well as ESR of the inductor apart from a host of other factors. It is essential, hence, to choose the right process, right architecture and the right external components to get the maximum efficiency possible.

For generating the 2.5V, depending on the current delivered, it may be possible either to use a linear regulator or a DCDC converter or a DCDC converter followed by a linear regulator. The first one is the cheapest solution and can be used in cases where the power delivered is low or performance is more premium than the power lost. The second one is more expensive, in that a switching regulator is used, though the efficiency would be good. This can be used in cases where a larger power supply noise can be tolerated but power loss is premium. In case both power lost and performance is premium, then the third option can be used, albeit at a higher price for the solution

Low footprint

With so many functions added in the device, the tight form factor leaves very little space for each of the functions. It is imperative that the power management function uses as low a footprint as possible. The power management footprint depends on the die size as well as the external components used. As noted earlier, it is essential that the right process be used to reduce the die footprint for a given configuration and performance. It is also essential to reduce the external component footprint. For switching converters, choosing architectures and switching frequencies impacts the value and hence the size of the inductors used. Architectures allowing use of a single inductor across multiple regulators also aid reducing the footprint needed. For Linear regulators, it is essential to keep the external capacitance at the output to a low value or if possible, eliminate it. In case an external capacitor is needed, the design should be able to work with smaller footprint capacitors, e.g. a 0402 form factor 1uF capacitor. These typically will show a lot of variation with voltage across it as well as with age. The size of the external components also depends on the load current profile. The larger the load transient, the larger the capacitor value requirements and hence more real estate.

DVM

One important aspect of power management is the control of voltage to the digital core. Depending on the processing power needed at any given time, the voltage to the device can be adjusted to consume the lowest amount of power needed. This is enabled by having the regulator adjust the voltage setting. Usually, it is good to have a 10mV resolution for these settings as it gives enough control over the voltage needed for a given processing power. Ability to control this dynamically from the digital core through a simple interface is critical for this.

Power Supply Current and Glitches

With multiple applications switching on and off based on either user requirement or system mandated, the power drawn from the battery varies a lot. Linear regulators typically present the load current to the battery as is and hence the current signature on the battery is mainly determined by the load. Most times, the linear regulators are used for analog circuits which typically take a constant current. Hence the load is not that much time varying. On the other hand, switching regulators, by design, present a switching current to the battery, even if the load current is a constant. This switching current causes the voltage on the power supply to

change. Keeping these glitches to a minimum depends on a lot of factors, like the power supply resistance, though important, is not in the direct control of the designers. Choosing the right decoupling capacitor and its placement is a critical factor. Architecture of the DCDC converter can help alleviate these issues. Using multiphase architecture for very high current DCDC converters are usually used. For medium to low current DCDC converters, it might be possible to use different phase of the clock to switch multiple DCDC converters. This tends to smooth the current profile presented to the supply.

Noise isolation for Analog / RF

Some of the analog circuits need a clean supply to ensure that their performance targets are met. This is usually accomplished by using a linear regulator with a good PSRR. It is essential to evaluate the PSRR requirement as a function of the frequency and well as the dropout voltage. Typically, higher the frequency, lower the PSRR. At low frequencies, the PSRR can be designed to a high value (~ 80db) rolling off to 40-50dB at 100's of KHz. Usually, beyond the Unity Gain Bandwidth (UGB) of the LDO (typically in a few MHz), the PSRR is determined by the capacitor at the output rather than the regulator itself. Also, as the difference between the output and input voltage of the regulator decreases, the PSRR falls due to fall in the gain of the regulator. Given the dependence of the PSSR on the conditions, it is essential to understand the usage scenario and choose the right regulator for this.

Apart from the supply noise, noise can be conducted to the sensitive circuits through the ESD ring and the substrate. Using isolation circuits in the ESD ring and guard rings help alleviate this issue.

Controllability

The ability to control the power supply based on the run time power consumption scenario aids in optimizing the power loss. This necessitates a simple communication protocol between the modules as well as sufficient programmability in the power modules themselves. While this works well once the system is booted up, startup presents a different case altogether. At startup, since the power is not up, the SoC or modules cannot control the Power management unit. The Power management unit has to come up autonomously based on set internal logic. Customization of this power sequence adds value to the unit as it can be customized to various systems.

Miscellaneous

Apart from the above, there are many other features that are needed in the system. Monitoring system parameters require an ADC, typically 10b with multiple channels. This can be used to either measure a voltage or a current flowing in some branch, based on which suitable action can be taken. An accurate Power On Reset and brown out monitor helps in monitor the systems health and take corrective actions if needed. Applications that need an accurate clock can use an XTAL oscillator circuit. Systems that can do with a 2% accurate clock, like many micro

controller applications, can save cost and pins by using a silicon oscillator. Displays and indication LEDs can be powered off an LED driver. Touch controllers can be integrated onto the system providing additional functionality to the system. Input and Output paths of the audio analog front ends can be integrated, making the system complete.

Components

Platform	**Features**
Buck Converter	High efficiency, low component value, programmable frequency, internal compensation
Linear Regulator	Capable of supporting high load current over wide output voltage, Low quiescent current
HV Boost Converter	High efficiency, Low component value, programmable frequency, internal compensation
Power Control Sub system	Input power Mux for AC adapter and USB, Battery Charger for Li-ion, Ni-Cd, Ni-Mh, Lead-Acid, Back up battery charger
Buck-Boost Converter	Auto transition, H bridge, low component value, internal compensation
Digital DVM Regulators	Small step size for output programming over wide range, low drop out, fast transient response, low quiescent current
Analog and RF LDOs	High PSRR up to high frequency of 1-2MHz, Low noise, Low Quiescent current
LED Diver	Buck converter and Boost converter for LED applications
Audio Codec	High performance A/D, D/A for high quality music, uPhone Amplifier, Class AB, Class D drivers with high output power and low quiescent current consumption
POR and precision voltage reference	Precision voltage reference, Power on reset and brown out indicators
Touch Screen controller	Resistive as well capacitive solutions
XTAL and Si Oscillators	Accurate clock reference using XTALs or 2% accurate clock reference using Si Oscillator

A case for PMASIC

Many of the functions listed above are primarily analog. While it may be possible to integrate these in DSM processes (and maybe some are better being integrated in the DSM SoC), the area doesn't shrink as it would for digital designs. Also the requirement to handle higher voltages,

say 7V, will complicate the design process in the DSM. This adds process complexity, increasing the cost of the whole solution. Putting all these in a separate analog optimized process will help in optimizing the performance as well as lowering cost. The industry has revolved around the 0.18um nodes for the optimized analog solutions. The combination of the ability to handle high voltages, optimized power transistors, availability of precision components and low costs have helped popularize these for power applications.

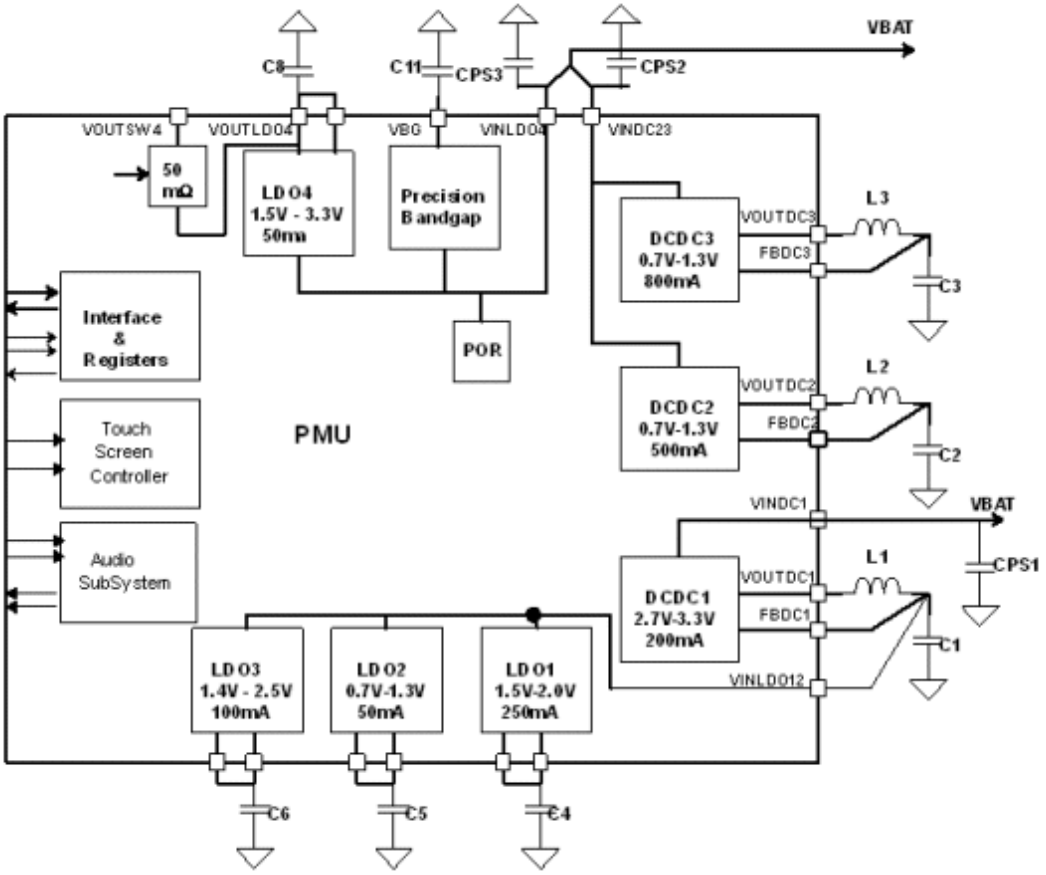

Figure 2: An Example PM ASIC

In addition, any custom feature that the system may require can be integrated in these devices. This extra level of flexibility will enable scaling of the digital SoC with the process nodes. And keep all the not-so-scaling friendly circuits in the analog companion chip. Not only will this help in cost optimization but also enable quicker turnaround for the system.

These analog companion function can be used either as a chip in the system or as a Known Good Die (KGD) in an MCM configuration.